10/619039

2825

501.36127CC3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Yasushi KOUBUCHI, ET AL.

10-619039

Serial No.: Rule 1.53(b) continuation of U.S. Patent Application Serial No.: 10/075,246, filed February 15, 2002

Filed: July 14, 2003

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, AND FABRICATION PROCESS AND DESIGNING METHOD THEREOF

Group of parent: 2825

Examiner of parent: Lee

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 AND §1.98

Mail Stop DD
Commissioner for Patents
P.O. Box 1450
Arlington, VA 22313-1450

July 30, 2003

Sir:

Pursuant to Applicants' duty of disclosure, enclosed please find a List of documents cited in prior application Serial No.: 10/075,246, filed February 15, 2002.

Since application Serial No. 10/075,246 is being cited under 35 U.S.C. §120 in the above-identified Continuation application, copies of the listed documents are not enclosed. See 37 CFR §1.98(d).

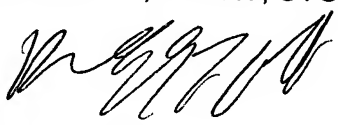
To the extent that the above-listed documents are not English, the requirements of 37 CFR §1.98(a)(3) are satisfied at least by the English translations enclosed with the documents as submitted in prior application Serial No.: 10/075,246.

In view of all of the foregoing, consideration of the listed documents, upon examination of the above-identified application, is respectfully requested.

Kindly charge any additional fees due, or credit overpayment of fees, to Deposit Account No. 01-2135 (501.36127CC3).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO.	SERIAL NO.
		501.36127CC2	10/619039
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT: KOUBUCHI, et al.	
		FILING DATE: July 10, 2003	GROUP: 2825

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
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	AN	07-092838	18-04-95	Japan			X	
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	AP	923844	6-2-97	Japan			Corres-ponding USP '736	
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	AR							
	AS							
	AT							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AU	Lee, et al., "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)", 1996, Symposium on VLSI Technology Digest of Technical Papers, pp. 158-159.
	AV	
	AW	
	AX	
	AY	
	AZ	

Examiner	Date Considered